

IBM Research partners with EU consortium to unleash the performance potential of mobile devices

The ACOTES project will help bring consumers a truly rich experience with power-intensive mobile applications such as video and interactive gaming,

Haifa Israel – January 07, 2008 – IBM recently joined EU partners for a review meeting of the ACOTES project, an EU funded initiative to maximize the potential of parallel computing in chips, while extending the battery life of consumer devices. Just some of the benefits this project will bring to consumers include longer lasting cell phones or the ability to watch TV on their mobile devices—without experiencing severe power drains.

“By getting more parts of the chip to work in parallel, we can bring new energy to mobile devices and redefine the power-performance ratio,” explained Harm Munk, ACOTES Project leader, Harm Munk, NXP Semiconductors, Corporate Research. “Rather than save battery life by reducing the power, ACOTES adds muscle to the chip’s computing power.”

Most chips today incorporate the ability to run computing tasks in parallel, but very few actually make use of the full performance potential available. If we could take a snapshot of a chip at work, we’d see that it contains both hot spots where computing is taking place, along with inactive areas that are not being used. ACOTES is geared towards helping chips reach a higher level of parallelism.

“Although the amount of parallelism built into the chips is increasing, it is also introducing greater complexity for application programmers who are now being challenged with expressing the parallelism and prioritizing the way computing tasks and resources should be allocated,” pointed out Dr. David Bernstein, manager of Software and Verification Technologies at the IBM Research Lab in Haifa. ACOTES tools and methodologies will make it easier to program and develop applications that take maximum advantage of the chip’s parallelism.

ACOTES partners are in the midst of a three-year program at the end of which, their new tools are expected to take advantage of 90% of chip parallelism for selected applications—as opposed to the 40 or 50% being utilized today. The tools developed will be made available to the open source community as part of the GCC compiler. The project consortium includes NXP Semiconductors (formerly Philips Semiconductors), the Netherlands; IBM Haifa Research Lab, Israel; STMicroelectronics, Switzerland; NOKIA, Germany; INRIA, France; Universitat Politècnica de Catalunya, Spain; and Silicon Hive.

Although previous attempts failed to create tools that automatically parallelized programs, ACOTES partners feel they’re on the right track. “We will first develop a robust methodology for working manually and then regulate its automation in a sure step-by-step process,” noted Munk. “We see this as a major first step that will shape an infrastructure upon which future projects and technologies can be built.”

The recent review meeting held in Paris was chaired by Javid Khan, ACOTES project officer from the European Commission in Bruxelles. The European Commission invited three experts from European universities and research center to act as external reviewers. The reviewers declared the project to be in very good shape and found the number and quality of the deliverables to be most impressive.

The IBM Haifa team working on ACOTES specializes in developing advanced optimizations for new compiler architectures for embedded systems. “Today’s power hungry devices need the ability to exploit chips’ full parallelism and new technological advances,” notes Bernstein. “Ultimately, real collaboration between industry, academia and the research community is the only way to bring true technology evolution to consumer devices.”
