

# Crosstalk Effect Minimization for Encoded Busses

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## Abstract

*In this paper we present a technique which allows to reduce the crosstalk-induced delay within busses implementing an error detecting/correcting code. This technique is based on the observation that the maximum delay on an encoded bus is usually due to the check bits that are added to provide the desired error detection/tolerance ability. These bits, in fact, are computed from the bus information bits by an ad hoc encoder, which adds an extra delay to the crosstalk-induced bus delay. We will show that, by proper placement of the lines carrying the information with respect to those carrying the check bits, it is possible to reduce the effective coupling capacitance due to the Miller effect among adjacent lines. This allows a reduction of propagation delay which, depending on the implemented code, can overcome the 20% with respect to the conventional placement of encoded busses.*

## 1. Introduction

The adoption of very deep submicron technologies (VDSM) poses new reliability and testing challenges, mainly due to the ICs' reduced internal node capacitances, power supply and noise margins [9, 2, 6].

As concerns busses, present (and future) technologies feature a sensible decrease of the inter-wire spacing. Wires are higher and closer one another, and consequently the mutual coupling capacitance is increasing compared with previous technologies. As a consequence, crosstalk effects are getting more and more relevant, and are becoming the main cause of noise and delay uncertainty within a bus [10, 1, 3]. In particular, if crosstalks affect the bus lines of a synchronous system, incorrect data may be sampled by the flip-flops (FFs) at the receiver side of the bus and propagated through the system, causing an incorrect behavior.

To satisfy the delay constraints and guarantee signal integrity, several techniques have been proposed, aimed at reducing the crosstalk-induced delay uncer-

tainty. The most common practices are: i) to insert repeaters [11, 12], and ii) to shield the wires [4]. Furthermore, it has been recently shown that, by introducing an intentional delay among coupled signal transitions, the crosstalk due delay can be reduced [5].

To face the problem of possible logic errors due to crosstalks, a fault-tolerant bus could be adopted. For instance, either error detecting codes followed by proper recovery, or error correcting codes could be implemented. The adoption of coding techniques implies the use of an encoder that, starting from the information bits, calculates the check bits. These generated check bits are, therefore, delayed with respect to the information bits by a time interval equal to the delay introduced by the encoder.

In this paper we present a technique which allows to reduce the maximum crosstalk-induced delay within busses implementing an error detecting/correcting code. It is based on the observation that the maximum delay on an encoded bus is usually due to the check bits, because of the extra delay added by their encoder to the crosstalk-induced bus delay. We will show that, by proper placement of the lines carrying the information with respect to those carrying the check bits, it is possible to reduce the effective coupling capacitance due to the Miller effect among adjacent lines, thus reducing the maximum bus delay. Our technique allows a reduction of the maximum bus delay that, depending on the considered code, can overcome the 20%, with respect to a conventional placement of encoded busses. Our analysis has been performed considering a realistic bus model, of the kind presented in [15].

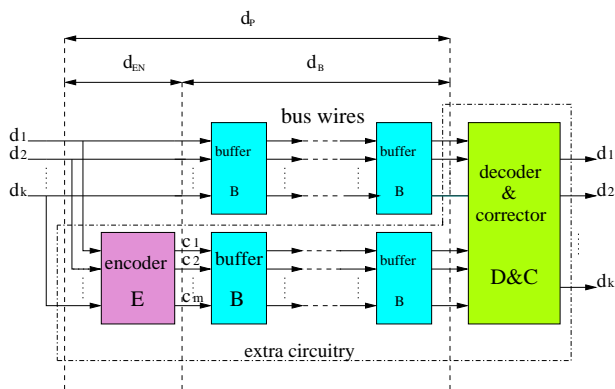
This paper is organized as follows. In Section 2, we recall the encoded bus general scheme and electrical model that we have employed for our analysis. In Section 3, we describe our proposed technique. In Section 4, we show its application to encoded busses and we report some of the results obtained by means of the electrical simulations that we have performed to verify the effectiveness of our technique. Finally, some conclusions are drawn in Section 5.

## 2 Considered Bus Encoding Scheme

A general scheme for bus encoding (using error correcting codes) is shown in Fig. 1. The  $k$  information bits to be transmitted are given to the inputs of an *encoder* (E), which adds  $m$  extra *check bits* to the information bits, thus obtaining codewords with the minimum Hamming distance  $d_{min}$  (i.e., the number of differing bit positions) that is required to achieve the desired degree of error correction (e.g.,  $d_{min} = 3$  for single error correction) [14, 13, 8]. These  $n = k + m$  bits are transmitted on the bus. At the other end of the bus, there is a circuit (*D&C* in Fig. 1), which detects and corrects the possible errors which might have occurred on the bus.

The *encoding* and *decoding* operations introduce a delay which depends on the code structure and on its error correction capability. For instance, for systems implementing a Hamming code, the encoder consists of a series of XOR trees (as many as the number of check bits), whose depth (and introduced delay) depends on the number of information bits. In particular, the *encoder* delays the check signals with respect to the information ones, thus making the transitions of the check bits non simultaneous with respect to those of the information bits.

As schematically shown in Fig. 1,  $d_{EN}$  represents the encoder input-output delay, whereas  $d_B$  is the bus delay. Therefore, the total delay, given by the sum of the encoder delay and the bus delay, can be written as:  $d_P = d_{EN} + d_B$ .



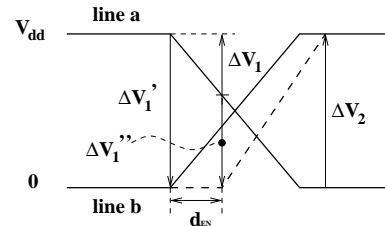
**Figure 1. General scheme for a bus with error correction.**

## 3 Basic Idea of the Proposed Technique

The crosstalk interference is caused by the inter-wire coupling capacitance ( $C_c$ ). The non simultane-

ous transition of adjacent wires causes a decrease of the crosstalk-induced bus delay with respect to the case of simultaneously switching adjacent wires, because of the reduction of the Miller effect.

In order to illustrate how non simultaneous transitions can allow a mutual effective capacitance reduction, in Fig. 2 we show two schematic transitions between two adjacent lines: a simultaneous transition (solid line) and a non simultaneous one (dashed line). For this latter, the transition of the *line b* is supposed delayed with respect to that of the *line a* by a time equal to a generic encoder delay ( $d_{EN}$ ). In particular, in the figure we have considered  $\Delta V = V_b - V_a$ , where  $V_a$  and  $V_b$  are the voltages on lines *a* and *b*, respectively.



**Figure 2. Schematic representation of two simultaneous and time shifted transitions.**

As for the case of simultaneous transitions, the effective capacitance between the two lines is given by:

$$C'_{eff} = \frac{\Delta V_2 - \Delta V_1'}{V_{dd}} \times C_c = \frac{V_{dd} - (-V_{dd})}{V_{dd}} \times C_c = 2C_c \quad (1)$$

while, for the non simultaneous transitions, we have:

$$\begin{aligned} C''_{eff} &= \frac{\Delta V_2 - \Delta V_1''}{V_{dd}} \times C_c = \frac{V_{dd} - (\Delta V_1' + \Delta V_1)}{V_{dd}} \times C_c \\ &= C'_{eff} - \frac{\Delta V_1}{V_{dd}} \times C_c \end{aligned} \quad (2)$$

It can be noticed that  $C''_{eff} \leq C'_{eff}$ , being  $\Delta V_1 \geq 0$ .

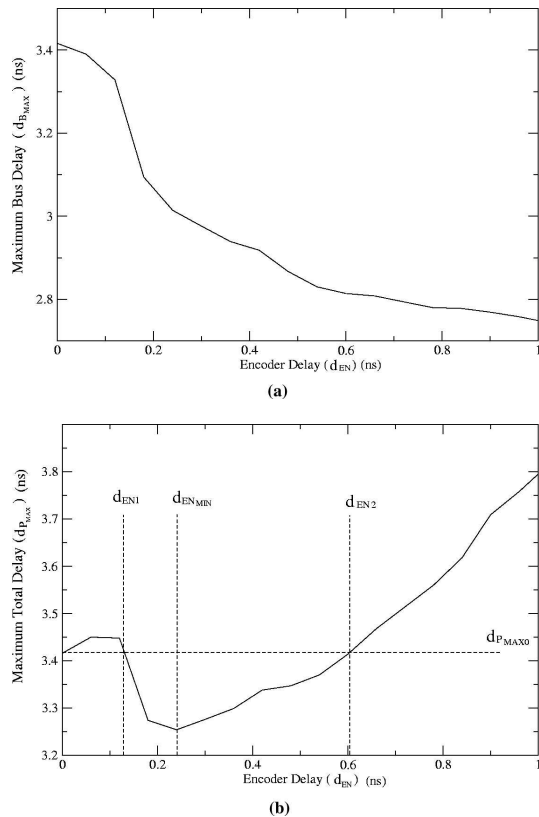
The voltage difference  $\Delta V_1$  depends on the delay  $d_{EN}$  between the two transitions and on the slope of *line a*, as indicated by the following equation:

$$\Delta V_1 = Sl_{line-a} \times d_{EN}, \quad (3)$$

where  $Sl_{line-a}$  is the slew rate of the *line a* and  $d_{EN}$  is the encoder delay.

Now let us analyze how the maximum and total bus delay change with the encoder delay ( $d_{EN}$ ). As an example, we have considered the case of a 3-wire bus, with the central line (*victim*) performing an opposite transition with respect to the adjacent lines (*aggressors*). The transition of the victim is shifted with respect to those of the aggressors by a time  $d_{EN}$ , which represents

the encoder delay. Each bus line (10mm long) has been divided into 5 equal segments by means of the insertion of repeaters. Each segment has been modeled by a  $\pi$  circuit, in order to better approximate a distributed  $RC$  bus line. The considered capacitance values correspond to the case of the minimum inter-wire spacing ( $= 0.21\mu m$ ) for the adopted  $0.13\mu m$  CMOS technology. Fig. 3(a) shows the bus delay of the central line, evaluated by means of electrical level simulations, as a function of  $d_{EN}$ . It represents the maximum bus delay (re-



**Figure 3. Maximum bus delay (a) and maximum total delay (b) as a function of the time shift ( $d_{EN}$ ) between the central victim line and the two aggressor lines.**

ferred as  $d_{B_{MAX}}$ ) since, for the considered transitions, the effective coupling capacitance for the central line is equal to its maximum value,  $4C_c$ . It can be noticed that  $d_{B_{MAX}}$ , as expected, decreases with the increase of  $d_{EN}$ , approaching a constant value, which for the considered example, is about  $2.75ns$ .

Fig. 3(b) shows the maximum total delay, given by  $d_{P_{MAX}} = d_{B_{MAX}} + d_{EN}$ . The value  $d_{P_{MAX0}}$  is the maximum total delay for  $d_{EN} = 0$  (i.e., when the transitions of the signals carried by adjacent lines are simultaneous). It can be noticed that the diagram can be di-

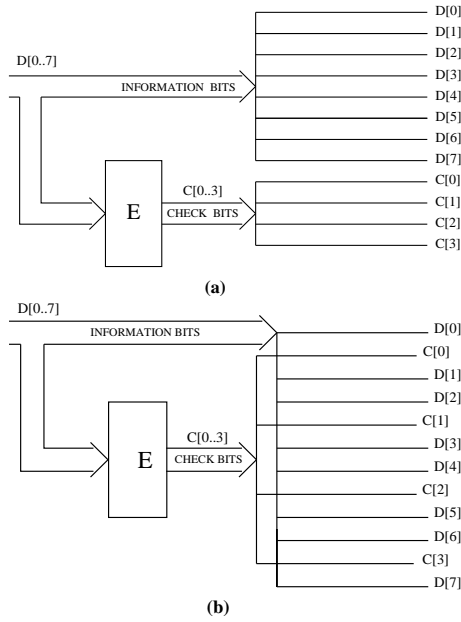
vided into three regions. In the first one, for  $0 \leq d_{EN} \leq d_{EN1} = 0.13ns$ , the maximum total delay ( $d_{P_{MAX}}$ ) is greater than  $d_{P_{MAX0}}$ . This is due to the fact that the decrease of the bus delay  $d_{B_{MAX}}$  is lower than the increase of the encoder delay  $d_{EN}$ . Hence, the maximum total delay, which is the sum of the encoder delay and the maximum bus delay, increases with respect to  $d_{P_{MAX0}}$ . For  $d_{EN1} = 0.13ns \leq d_{EN} \leq d_{EN2} = 0.6ns$  the maximum total delay is lower than  $d_{P_{MAX0}}$ : in this region, the values of the encoder delay allow a reduction of the voltage difference of the adjacent wires and consequently the inter-wire effective capacitance is smaller. This fact implies a decrease of the maximum total delay. Furthermore, it is worth noticing that  $d_{P_{MAX}}$  reaches a minimum value for  $d_{ENMIN} = 0.24ns$ . For values of  $d_{EN}$  greater than  $d_{EN2}$ , the maximum bus delay  $d_{B_{MAX}}$  slightly varies, since there is no further effective inter-wire capacitance reduction, while the maximum total delay increases almost linearly with the increase of  $d_{EN}$ .

#### 4 Application to Encoded Busses and Obtained Results

Usually, in a conventional encoded bus structure there are  $k$  adjacent wires carrying the data, followed by  $m$  wires carrying the check bits. As an example, in Fig. 4(a) we show the case of a bus encoded using a  $SEC$  Hamming code, with  $k = 8$  and  $m = 4$ .

Based on the considerations introduced in Section 3, we propose a new bus scheme in which the information signals and the check signals are alternatively placed on adjacent wires. In this way, the signals carried by adjacent wires will not switch simultaneously, since the check signal transitions are delayed (with respect to those of the information ones) of a delay equal to that of the encoder. Since the number of check signals is generally less than that of the information signals, it is always possible to place each wire, carrying a check signal, between two wires carrying the information signals. Consequently, it is always possible to exploit the reduction of the Miller effect due to the non simultaneous transitions in order to achieve a reduction of the maximum delay caused by crosstalk. As an example, Fig. 4(b) shows a possible bus structure which exploits the proposed idea. As can be seen, two consecutive check signals are separated by two data signals. However, it has been verified that placing a different number of data signals between two consecutive check signals, the obtained results are almost the same.

To estimate the propagation delay through the bus, we have to consider all transitions between possible signal patterns. As previously stated, the maximum delay

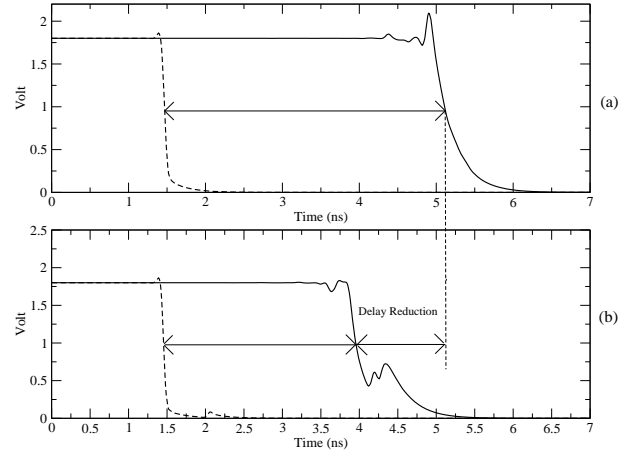


**Figure 4. Example of a traditional bus scheme for a 8 bit information system encoded by the Hamming code.**

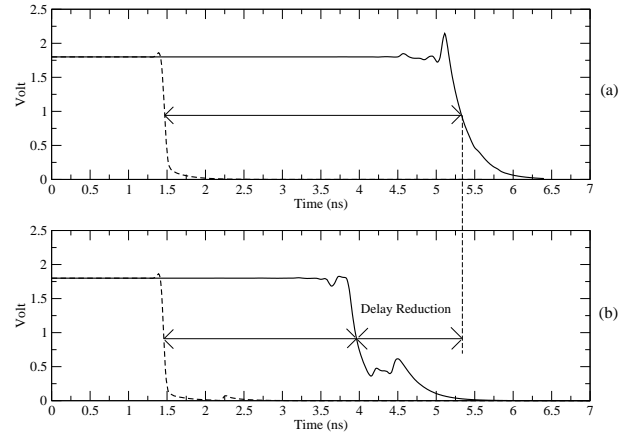
for a victim line occurs when both the adjacent wires switch simultaneously in opposite directions. For both a conventional and our proposed bus structure, the maximum total delay concerns the check signals, because of the encoding operation.

For the proposed bus configuration, the crosstalk effect on a delayed wire (check signal) is smaller than that of a conventional case, resulting in a bus delay reduction. The reason for the maximum bus delay reduction is that the time shift between adjacent wires, introduced by the encoding circuit, limits the Miller effect and consequently reduces the value of the effective capacitance of a delayed wire.

To verify the effectiveness of our proposed technique, we have performed electrical level simulations by means of HSPICE, modeling the bus as introduced in Section 3. The encoder delay, for a 8 bit information system using a Hamming code, is  $600ps$ . For such a system, Fig. 5 (a) shows the waveforms of the input (dashed line) and of the output (solid line) of a check signal which experiences the worst case delay, in the case of traditional bus wire placement. Similarly, in Fig. 5 (b) we show the waveforms of the analogous signal in the case of the adoption of our proposed bus configuration. The maximum total delay is  $4.12ns$ , but it falls to  $3.34ns$  by using our proposed technique. Therefore, we can achieve a 18% maximum delay reduction with respect to the conventional encoded bus placement.



**Figure 5. Voltage Waveforms at the beginning and end of a bus line in the case of (a) a traditional bus scheme (b) our proposed scheme for a (12,8) SEC Hamming code.**



**Figure 6. Voltage waveforms at the beginning and end of a bus line in the case of a) traditional bus scheme b) our proposed scheme for a (38,32) SEC Hamming code.**

In Fig. 6 we show the same waveforms of Fig. 5, but considering a code whose encoder consists of 4 XOR gate levels (for instance, the (22,16) SEC-DED Hamming Code). We can see that our technique allows a performance improvement of the 20%.

In Tab. 4 we report the values of the maximum total delay reduction, evaluated considering the worst case transition, achievable using the proposed structure for different error correcting codes and number of information bits. It can be noticed that, using the proposed

scheme, we obtain a delay decrease with respect to the conventional bus placement that varies from the 18%, when a (11,8) SEC, or (21,16) SEC, or (12,8) SEC-DED Hamming code is adopted, to the 21%, when a SEC or SEC-DED code for 64 data bits is employed.

It should be noted that our scheme can be applied to any bus implementing a systematic code, thus featuring intrinsically delayed check signals compared to the information ones. In fact, modifying the bus placement by alternating the information and check lines, we can reduce the Miller effect impact and, consequently, the effective capacitance between adjacent lines. In this way, the delay introduced by the encoding circuit (anyway present in systems with separable codes) can be exploited to reduce the bus lines' delay caused by the coupling capacitance between adjacent wires.

**Table 1. Percentage of maximum total delay reduction, obtained with our proposed scheme with respect to traditional bus schemes.**

Code Type	Data Bit Number	Check Bit Number	Delay Reduction
SEC	8	4	18%
SEC-DED	8	5	18%
SEC	16	5	18%
SEC-DED	16	6	20%
SEC	32	6	20%
SEC-DED	32	7	20%
SEC	64	7	21%
SEC-DED	64	8	21%

## 5 Conclusions

In this paper we presented a new scheme which allows to reduce the maximum crosstalk-induced delay within VDSM busses using an error detecting/correcting code. In particular, we showed that, by proper alternation of the lines carrying the information bits with those carrying the check bits, we can reduce the effective coupling capacitance due to the Miller effect between adjacent lines, thus reducing the maximum bus delay.

The results of the performed HSPICE simulations showed that our scheme allows a 18% maximum delay decrease for a 16 bit data system implementing a Hamming code, and a 20% decrease for a 32 bit data system using a SEC-DEC code, with respect to conventional bus configurations.

Our scheme can be applied to any bus implementing a systematic code and provides a way to exploit the

delay introduced by the bus encoding circuit in order to reduce VDSM bus lines' delay due to the capacitive coupling between adjacent wires.

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