

# Transient Performance of Common Modeling Assumptions Used in Detailed Thermal Package Models

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## ABSTRACT

Thermal conduction models of chip packages that include every geometric detail are impractical for use in the product design process. Detailed thermal models used for design employ a number of geometric simplifications that have been well validated for steady state analyses. This paper investigates the performance of these simplifying assumptions in the transient domain, where little validation of their performance exists. The results of the investigation show these modeling assumptions give the correct transient behavior.

The impact of their use within the model of an actual package was also investigated by comparing models built with and without these assumptions in different finite software tools, which again showed they give the correct transient behavior. These results are important for system designers undertaking transient analyses at the board and system level, and for those creating transient compact thermal models.

## Introduction

Whereas it is possible to build a thermal conduction model of a package including every detail of its construction, including individual traces in a BGA substrate [1], it is neither practical nor desirable to use such models for design calculations at the board or system level. Detailed thermal models used for design generally embody a number of simplifications that greatly reduce the geometric complexity of the model whilst having little impact on the quality of the results [2]. Such modeling

assumptions have been used for steady state analyses for a number of years [3, 4]

This paper presents a fundamental investigation into the performance of these simplifying assumptions in the transient domain using the finite volume (FV) computational fluid dynamics (CFD) tool FLOTHERM. Their performance within two actual packages is also investigated by comparing models built with these assumptions in the CFD tool with models built without these assumptions in two different finite element (FE) tools, ANSYS and MARC.

## Fundamental Investigations

### 1. Collapsed Die Attach Representation

#### 1.1 Model Details

The influence of treating the die attach as a 2-D plate, in which its thermal mass is ignored, was investigated by comparing this with a 3D representation of the die attach. Details of the geometry, including detail of the 3D representation of the die attach is shown below:

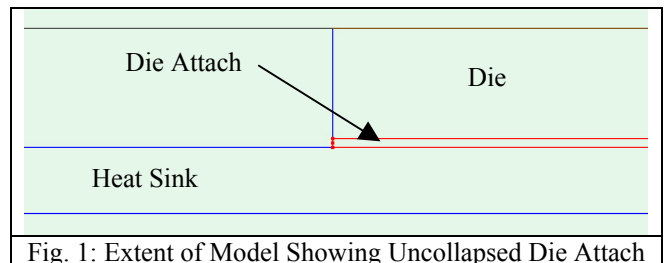


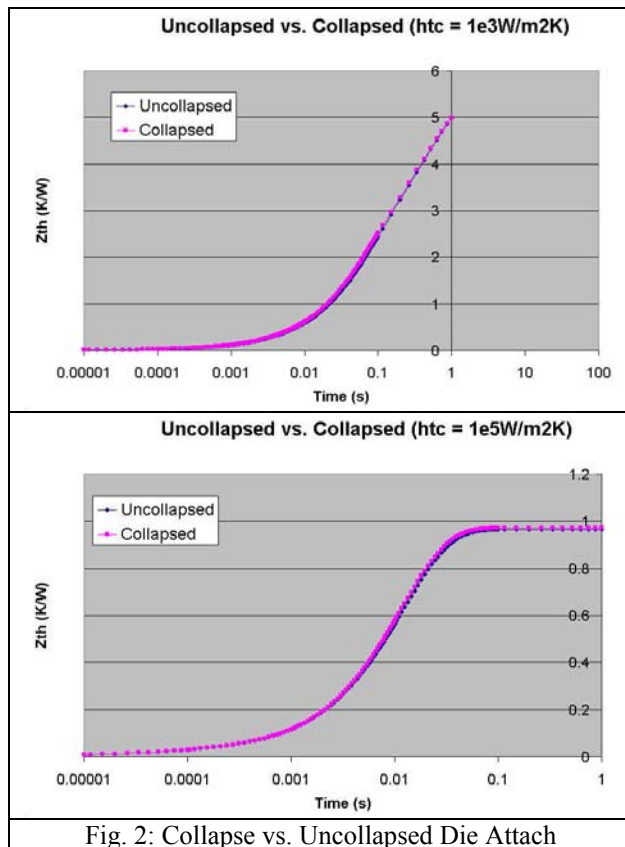
Fig. 1: Extent of Model Showing Uncollapsed Die Attach

The model consists of a 10mm x 10mm x 0.25mm silicon die mounted on a 40mm x 40mm x 1.5mm copper heat sink. The thickness of the die attach epoxy was 0.02mm. In the collapsed case, the thickness of the die was increased by the die attach thickness. In an actual package this treatment preserves the location of the top surface of the die within the model and hence the thickness of the package material above, thereby having the least effect on the thermal resistance of the assembly. Typical thermal properties were used for all materials.

A planar heat source of 2W was applied uniformly over the top surface of the silicon die, and heat transfer coefficients of  $1 \times 10^3 \text{W/m}^2\text{K}$ ;  $1 \times 10^4 \text{W/m}^2\text{K}$ ; and  $1 \times 10^5 \text{W/m}^2\text{K}$  were applied to the bottom surface of the copper substrate to represent the heat sinking of the board under the package. The ambient was  $0^\circ\text{C}$ . A quarter model was used due to symmetry. A steady state grid refinement study was performed to establish mesh independence, and a  $47 \times 47 \times 40$  mesh was chosen for the transient analysis. The time grid is indicated by the points shown on the graphs below. All time steps were converged down to the round off error of the machine.

## 1.2 Results

The graphs below show the temporal response for the center of the heat source for the highest and lowest heat transfer coefficients.



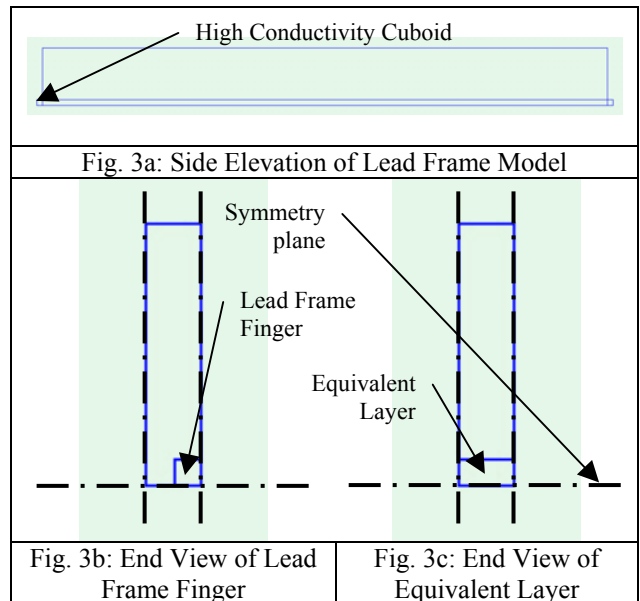
## 1.3 Discussion of Results

The results above show that the thermal behavior of the two models is nearly identical, with the collapsed case showing the slightly higher temperatures due to the higher thermal resistance of the die. As such this approximation seems acceptable provided the thickness of the die is relatively large compared to that of the die attach.

## 2 Averaged Lead Frame Representation

### 2.1 Model Details

The influence of using a lumped mass approximation for the lead frame region was investigated by comparing a detailed 3D representation of a single lead frame finger surrounded by plastic encapsulant with that of a thermally equivalent layer. A unit cell approach was taken, with half a lead frame finger, plus half the adjacent encapsulant included in the model, with a symmetry condition applied on these faces. Encapsulant above and below the lead frame was included, and again symmetry employed to allow just the top half of the package to be modeled. Details of the geometry and the symmetry conditions used are shown below.



As shown in Figure 3a, two high conductivity cuboids with very low thermal mass are included at the ends of the lead frame region to apply the heat source at one end of the model and an imposed heat transfer coefficient at the other. Excluding these objects, the length of the model was 10mm. The height and width of the model were 1mm and 0.2mm respectively. The lead frame coverage,  $\alpha$ , was 0.5. The material properties of the layer were calculated as follows:

$$k_{Effective} = \alpha k_{Copper} + (1 - \alpha)k_{Plastic}$$

$$\rho_{Effective} = \alpha\rho_{Copper} + (1 - \alpha)\rho_{Plastic}$$

$$Cp_{Effective} = \frac{\alpha\rho_{Copper}Cp_{Copper} + (1 - \alpha)\rho_{Plastic}Cp_{Plastic}}{\rho_{Effective}}$$

Heat transfer coefficients of  $1 \times 10^4 \text{W/m}^2\text{K}$ ;  $1 \times 10^5 \text{W/m}^2\text{K}$ ; and  $1 \times 10^6 \text{W/m}^2\text{K}$  were used to represent the heat sinking of the board around the lead. A heat transfer coefficient of  $20 \text{W/m}^2\text{K}$  was used on the top of the encapsulant and a heat source of  $0.025 \text{W}$  was applied at the start of the transient. The ambient was  $0^\circ\text{C}$ . A grid refinement study was performed. Identical grids were used for the detailed and compact models. The final grid had  $128 \times 22 \times 10$  cells in the length, height and width directions. Again, the time grid is shown on the graphs below. All time steps were fully converged.

## 2.2 Results

The graphs below show the temporal response of the temperature of the heat source for the highest and lowest heat transfer coefficients.

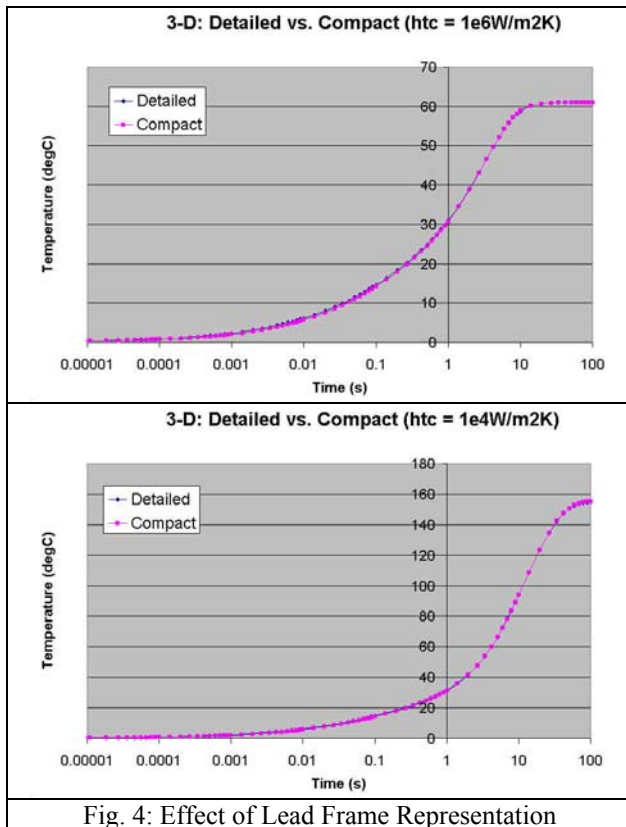


Fig. 4: Effect of Lead Frame Representation

## 2.3 Discussion of Results

The results show that the thermal behavior of the two models is nearly identical. As such this approximation also seems highly acceptable.

## Package Model Studies

Two package model studies were undertaken. The first considers a 352-BGA part, and the second a 80-PQFP. Both packages have been investigated as part of the PROFIT project (Prediction of Temperature Gradients Influencing the Quality of Electronic Products), [5, 6]. Both packages are mounted in a Double Cold Plate (DCP) fixture, with spacers used to contact the package to the cold plates. For readers not familiar with the DCP approach [7], it exercises different heat from paths from the package surfaces as described in the table below.

Table 1: Heat Flow Path by DCP Configuration

	Preferential heat flow path exercised
DCP-1	Top and bottom of package
DCP-2	Bottom of package
DCP-3	Top of package
DCP-4	Package interconnect (leads / solder balls)

## 3 HBGA352 in DCP-1 Configuration

### 3.1 Model Details

The package is a thermally enhanced wire bonded die down PBGA with an exposed copper heat slug (Viper BGA). The geometry of the model is shown in Figure 5. The package consists of a  $35 \text{mm} \times 35 \text{mm} \times 0.381 \text{mm}$  copper stiffener onto which a  $15.12 \text{mm} \times 15.12 \text{mm} \times 0.38 \text{mm}$  silicon die is attached with a  $85 \mu\text{m}$  glue layer. Beyond the edge of the die adhesive is used to attach the material stack-up comprising the BGA substrate. The die and part of the BGA substrate is overmolded with epoxy. The package termination is via four rows of Sn63/Pb37 solder balls on a  $1.27 \text{mm}$  pitch.

Effective material properties were calculated for the inner and outer regions of the PCB in the BGA substrate, taking the proportions of copper in these regions 0.19 and 0.1 respectively using the formulae given in the section above. The thermal conductivity of the silicon was treated as temperature dependent. Convection and radiation from the exposed surfaces are ignored in the modeling.

The temperatures of the cold plates rise over the duration of the transient from their initial value of  $25^\circ\text{C}$  due to the high power being used. However, it was not possible to include this information in the modeling as the thermal response of the cold plates was not measured during the experiment.

A detailed grid refinement study was performed. Identical grids were used for the detailed and compact models. The final grid used was the  $62 \times 62$  in the plane of the package and 40 cells through the pedestals and package, with grid cells concentrated within the package. Again, the time grid is indicated by the points on the graphs below, and all time steps were converged down to the round off error of the machine.

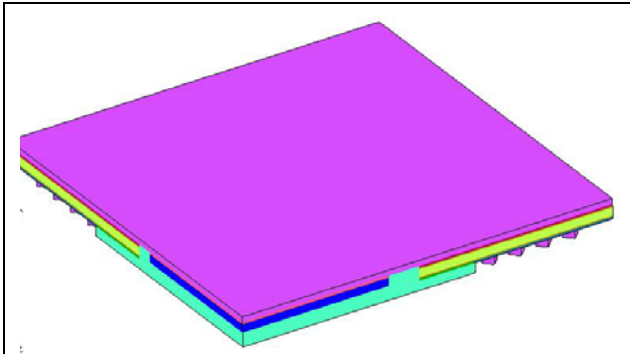


Fig 5a: Isometric of FE Package Model

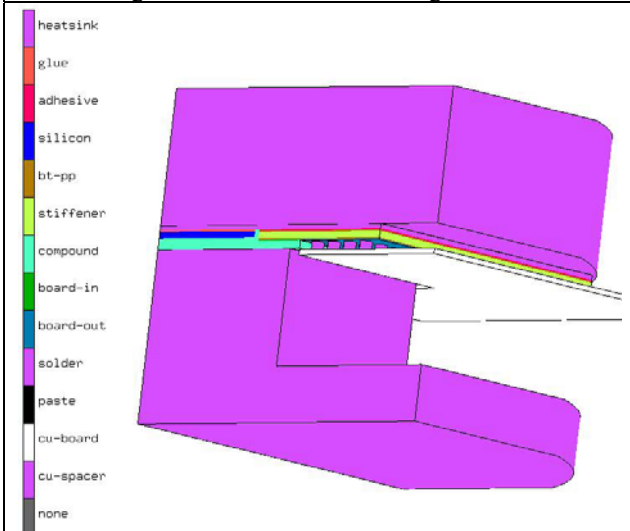


Fig 5b: Isometric of FE Model in DCP-1

### 3.2 Results

A heat transfer coefficient of 5000W/m<sup>2</sup>K was used to represent the cold plate contact with the pedestals. The full package power was 55.85W. The top cold plate was at 29°C, and the bottom cold plate at 26.3°C, being the values measured at the end of the experiment. These boundary conditions are identical to those used by Philips.

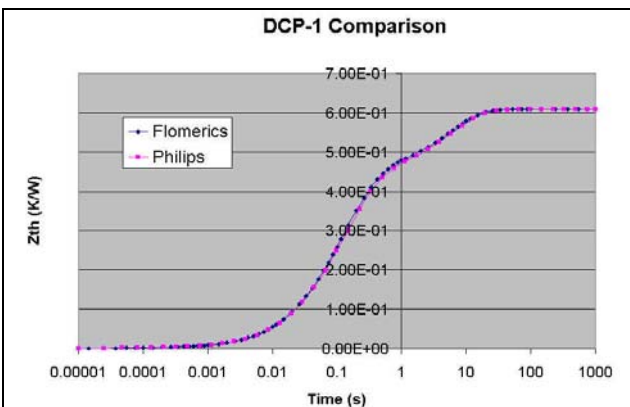


Fig. 6: Comparison of FE and FV Models

The results are reported in terms of a thermal resistance,  $Z_{th}$ , defined as:

$$Z_{th} = (T_J - T_{CP}) / P$$

where  $T_J$  is the temperature at the center of the die heat source,  $T_{CP}$  is the temperature of the cold plates, and  $P$  is the full model applied power.

### 3.3 Discussion of Results

The results show excellent agreement between the two software tools. This is to be expected, since both the geometric models were very similar, modeling all objects as conducting cuboids. In the FE tool, the solder balls were modeled at 45° to the axes of the model.

A significant departure from the experimental results was observed around 0.5s after which time the boundary conditions start to influence the results. Some discrepancy between the numerical and experimental results occurred after around 0.01s, arising from uncertainties in the material property data used in the modeling.

## 4 P-MQFP-80-1 in DCP-1 to DCP-4

### 4.1 Model Details

The geometry of the model is shown in Figure 7 below.

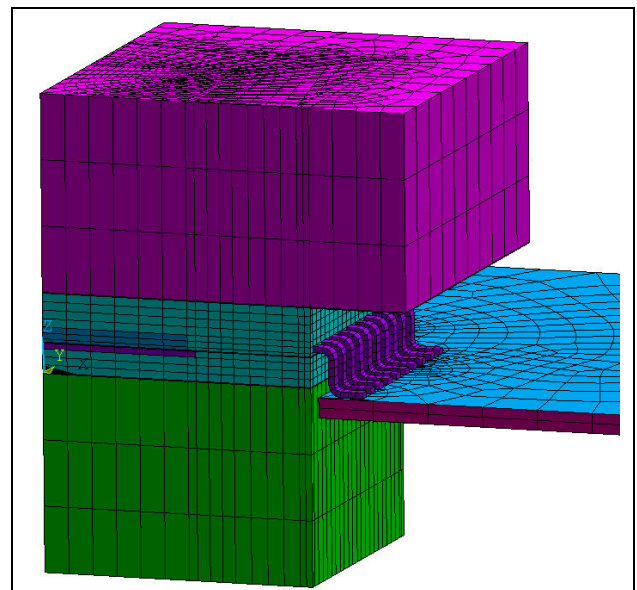
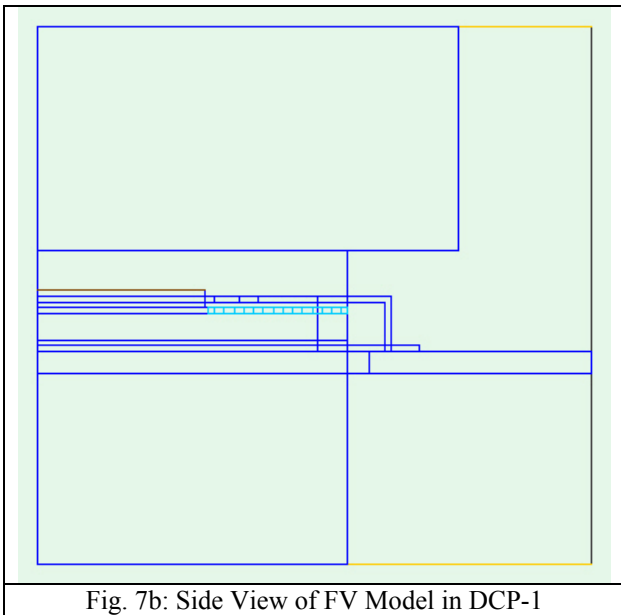


Fig. 7a: Isometric of FE Model in DCP-1

Lack of space prevents the inclusion of full geometric details and material properties used in the analysis. However, the main details are as follows: The package body is 14mm x 14mm x 2.25mm encapsulant and contains a 7.56mm x 7.56mm x 0.38mm silicon die

mounted on a 8mm x 8mm x 0.15mm copper alloy die pad with a 20 $\mu$ m thick glue die attach. The die attach was treated as thermally 'thin', being modeled as a 2-D plate. Consequently its thermal mass was not included in the calculation. The metal coverage in the lead frame region was 66%. The leads on each side of the package were soldered to a 25mm x 10mm x 0.5mm thick copper strip. Averaged material properties were used for the lead frame region, and the external leads. The thermal conductivity of the silicon was treated as temperature dependent. In the FE model, the heat capacity of the silicon was also treated as temperature dependent. This feature is not available in the FV software. Convection and radiation from the exposed surfaces are ignored in the modeling, as Infineon found these to have a negligible influence on the results.



The die attach was collapsed and its thickness in the model added to that of the die, increasing the die thickness from 0.38mm to 0.382mm. This was compared with a non-collapsed die attach for the DCP-2 and DCP-3 analyses, which respectively extract heat through the bottom (via the die attach) and top of the package.

A steady state grid refinement study was performed to establish mesh independence of the results, and the mesh used for the transient analysis had 111 x 117 cells in the plane of the package and 51 cells through the pedestals and package, with grid cells concentrated within the package. Again, the time grid is indicated by the points on the graphs below, and all time steps were converged down to the round off error of the machine.

The sensitivity of the modeling results to the representation of the lead frame finger to die pad gap was also assessed. The diagram below shows a plan view of the package and the surrounding copper strips. The tie bars extend from the corner of the die pad to the corner of

the package body. The exact shape of the gap is formed by the inclusion of the two prisms.

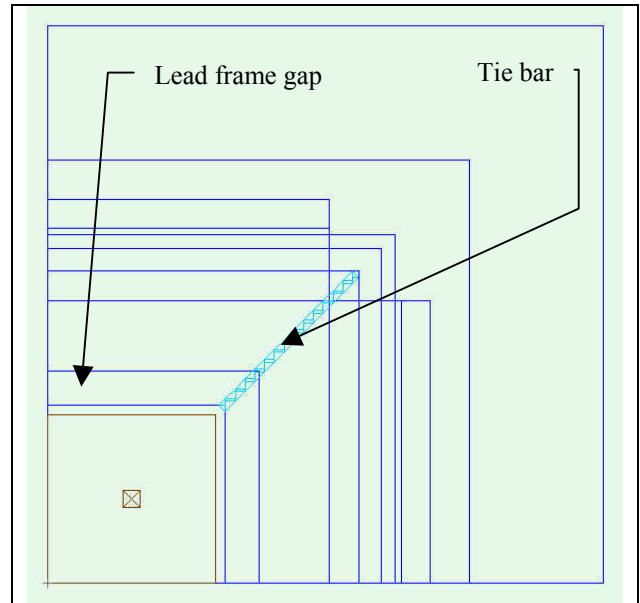


Fig. 8a: Plan View of FV Model, Average Gap

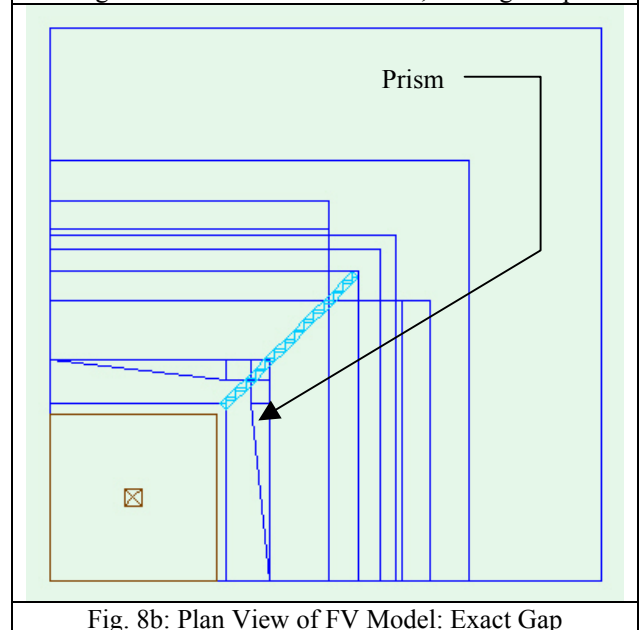


Fig. 8b: Plan View of FV Model: Exact Gap

## 4.2 Results

The full package powers used for each DCP configuration are given in Table 2.

**Table 2: Powers used in the FV Analysis**

DCP Configuration	Full Model Power (W)
DCP-1	6.3
DCP-2	3.7
DCP-3	3.9
DCP-4	1.8

The initial condition used was a uniform temperature of 25°C. The results are reported in terms of a thermal resistance, so the results should be largely insensitive to the powers used. Infineon used a power of 5W for the FE modeling of all DCP configurations. For DCP-1 to DCP-3, a heat transfer coefficient of 10000W/m<sup>2</sup>K was used to represent the contact between the pedestals and the cold plates, which were assumed to be at 25°C. For both pedestals an oil film thickness of 5µm was used for DCP-1 & 3, and 20µm for DCP-2.

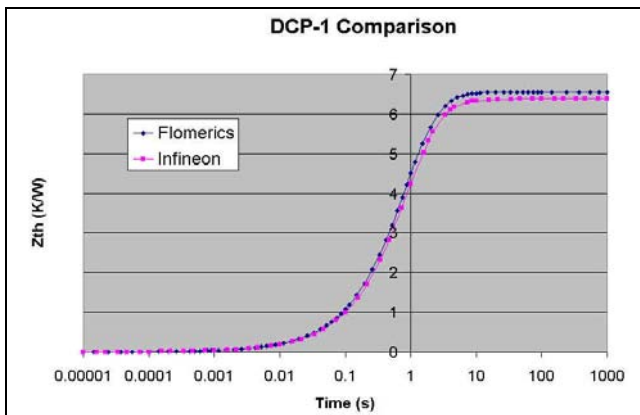


Fig 9a: FE vs. FV Analysis for DCP-1

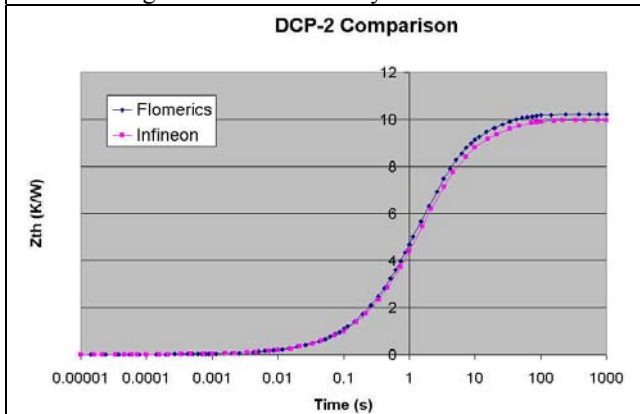


Fig. 9b: FE vs. FV Analysis for DCP-2

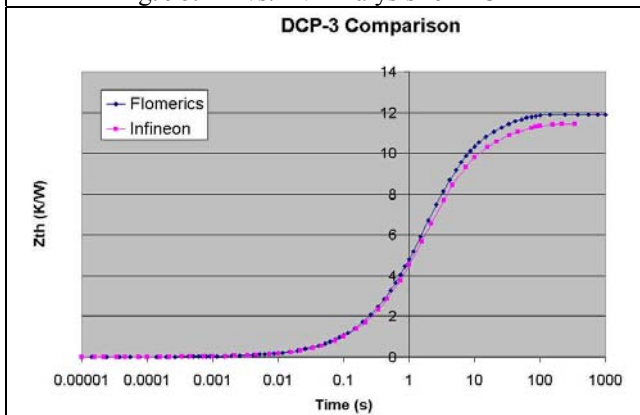


Fig 9c: FE vs. FV Analysis for DCP-3

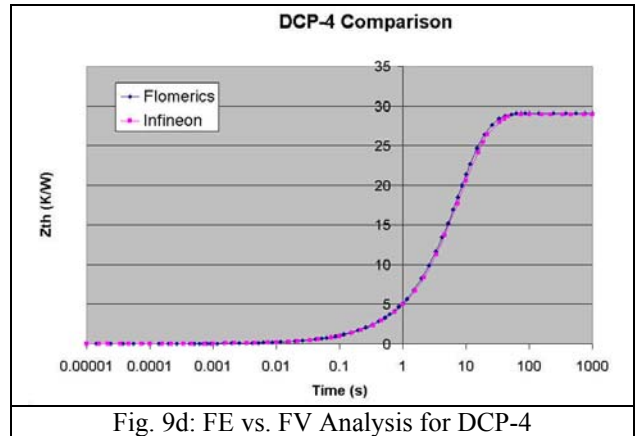


Fig. 9d: FE vs. FV Analysis for DCP-4

For DCP-4 a heat transfer coefficient of 10000W/m<sup>2</sup>K was applied to the bottom of the copper sheets to represent their contact to the lower cold plate. No oil film was included in the DCP-4 configuration, as the effect of this is incorporated in the heat transfer coefficient applied to the underside of the copper sheets. An oil film thickness of 10µm is equivalent to a heat transfer coefficient of 14000W/m<sup>2</sup>K.

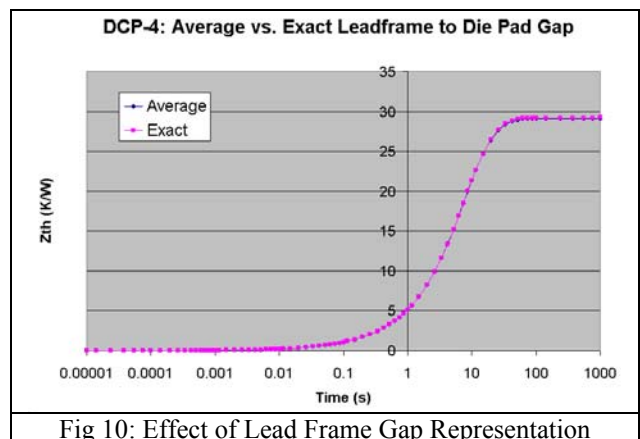


Fig 10: Effect of Lead Frame Gap Representation

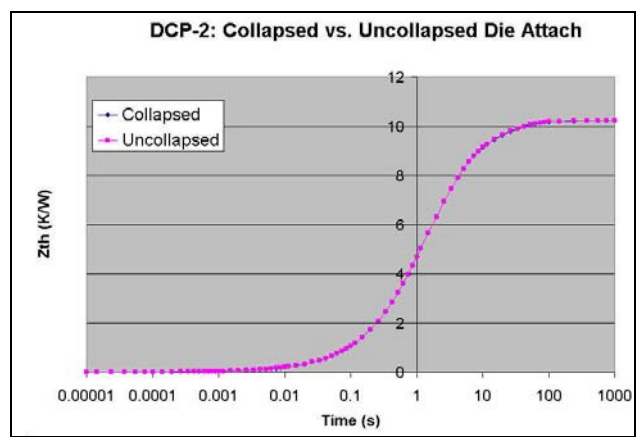


Fig 11: Effect of Die Attach Representation (DCP2)

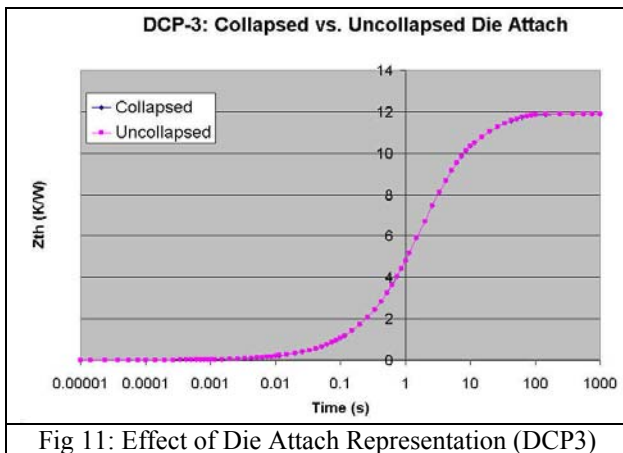


Fig 11: Effect of Die Attach Representation (DCP3)

### 4.3 Discussion of Results

Figures 10 and 11 show that the model is insensitive to the representation of the die attach and the lead frame gap, consistent with the results of the fundamental studies performed. Figure 9d shows excellent agreement for DCP-4, where the heat is primarily removed from the leads. Figures 9a to 9c show poorer agreement for DCP-1 to DCP-3. Since the fundamental studies have shown this is not due to the modeling assumptions employed in the FV model, this difference in results must be attributed to other differences between the models. The most significant difference is the geometric representation of the tie bar. This is correctly represented in the FE model, being bent up from the corner of the die pad to into the plane of the lead frame. In the FV model the tie bar simply protrudes from the corner of die pad and is not bent up into the plane of the lead frame, as shown in Figure 7b. However, comparison with a more detailed tie bar representation in the FV model eliminated this as the cause of the discrepancy. Further study is needed to establish the cause of the discrepancy. However, it should be noted that the differences between the two models are less than the differences measured between different physical parts [8].

### Conclusions

The modeling assumptions generally used in the creation of steady state detailed thermal model of chip packages have been shown to work equally well in the transient domain. This is an important conclusion for system designers undertaking transient analyses at the board and system level, as well as those creating transient compact thermal models [9, 10].

### Acknowledgements

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ordinated by Philips Research. The project consortium includes semiconductor manufacturers (Philips Semiconductors, Infineon Technologies, ST Microelectronics); system makers (Nokia, Philips); thermal analysis software vendors (Flomerics, MicRed); a statistics expert centre (Centre for Quantitative Methods); a university specializing in electrothermal analysis and transient measurements (Technical University of Budapest); and a major research institution contributing in the fabrication of test dies and tool integration (TIMA).

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